WHAT IS CLAIMED IS:

1. A decoder for use in wordline/bitline redundancy control, comprising:

first and second wordlines configured to be activated based on decoded first and second addresses;

redundant first and second wordlines respectively coupled to the first and second wordlines; and

first and second shift registers respectively coupled to the redundant first and second wordlines and configured to respectively activate the redundant first and second wordlines when the first or second wordlines contain a defect.

2. The decoder as recited in Claim 1, further comprising first and second wordline drivers respectively coupled to the first and second wordlines and configured to activate the first and second wordlines when the first or second wordlines are free of defects.

3. The decoder as recited in Claim 2, further comprising first and second steering circuits respectively coupled to the first and second wordline drivers and configured to select a signal to cause the first and second wordline drivers to activate the first and second wordlines.

4. The decoder as recited in Claim 3, further comprising first and second logic gates respectively coupled to the first and second steering circuits and configured to provide the decoded first and second addresses.

5. The decoder as recited in Claim 1, further comprising redundant first and second wordline drivers respectively coupled to the redundant first and second wordlines and configured to activate the redundant first and second wordlines when the first or second wordlines contain a defect.

6. The decoder as recited in Claim 5, further comprising redundant first and second steering circuits respectively coupled to the redundant first and second wordline drivers and configured to select a signal to cause the redundant first and second wordline drivers to activate the redundant first and second wordlines.

7. The decoder as recited in Claim 1, wherein the first and second wordlines are odd and even wordlines, respectively, and the redundant first and second wordlines are redundant odd and even wordlines, respectively.

8. A method of selecting wordlines for use in wordline/bitline redundancy control, comprising:

coupling first and second wordlines to respective redundant first and second wordlines, the first and second wordlines configured to be activated based on decoded first and second addresses; and

activating the redundant first and second wordlines, using first and second shift registers coupled to the respective redundant first and second wordlines, when the first or second wordlines contain a defect.

9. The method as recited in Claim 8, further comprising coupling respective first and second wordline drivers to the first and second wordlines and to activate the respective first and second wordlines when the first or second wordlines are free of defects.

10. The method as recited in Claim 9, further comprising selecting a signal, using first and second steering circuits coupled to the respective first and second wordline drivers, to cause the first and second wordline drivers to activate the first and second wordlines.

11. The method as recited in Claim 10, further comprising providing the decoded first and second addresses using first and second logic gates coupled to the respective first and second steering circuits.

12. The method as recited in Claim 8, further comprising activating the first and second redundant wordlines using redundant first and second wordline drivers coupled to the respective redundant first and second wordlines when the first or second wordlines contain a defect.

13. The method as recited in Claim 12, further comprising selecting a signal, using redundant first and second steering circuits coupled to the respective redundant first and second wordline drivers, to cause the redundant first and second wordline drivers to activate the redundant first and second wordlines.

14. The method as recited in Claim 8, wherein coupling first and second wordlines to respective redundant first and second wordlines includes coupling odd and even wordlines to respective redundant odd and even wordlines, and activating the redundant first and second wordlines using first and second shift registers, and comprises activating the redundant odd and even wordlines using odd and even shift registers.

15. A wordline decoder having redundancy control capabilities, comprising:
circuitry comprising an initial wordline decode stage; and
circuitry comprising a final wordline decode stage, comprising:
circuitry comprising first and second wordlines coupled to respective redundant first and second wordlines, each first and second wordlines configured to be activated based on decoded first and second addresses; and
circuitry comprising first and second shift registers coupled to the respective redundant first and second wordlines and each configured to activate the respective redundant first and second wordlines when the first or second wordlines contain a defect.

16. The decoder as recited in Claim 15, further comprising first and second wordline drivers coupled to the respective first and second wordlines and configured to activate the first and second wordlines when the first or second wordlines are free of defects.

17. The decoder as recited in Claim 16, further comprising first and second steering circuits coupled to the respective first and second wordline drivers and configured to select a signal to cause the first and second wordline drivers to activate the first and second wordlines.

18. The decoder as recited in Claim 17, further comprising first and second logic gates coupled to the respective first and second steering circuits and configured to provide the decoded first and second addresses.

19. The decoder as recited in Claim 15, further comprising redundant first and second wordline drivers coupled to the respective redundant first and second wordlines and configured to activate the redundant first and second wordlines when the first or second wordlines contain a defect.

20. The decoder as recited in Claim 19, further comprising redundant first and second steering circuits coupled to the respective redundant first and second wordline drivers and configured to select a signal to cause the redundant first and second wordline drivers to activate the redundant first and second wordlines.